

An Empirical Guide to the Behavior and Use of Scalable Persistent Memory

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Abstract

After nearly a decade of anticipation, scalable nonvolatile memory DIMMs are finally commercially available with the release of Intel’s 3D XPoint DIMM. This new nonvolatile DIMM supports byte-granularity accesses with access times on the order of DRAM, while also providing data storage that survives power outages.

Researchers have not idly waited for real nonvolatile DIMMs (NVDIMMs) to arrive. Over the past decade, they have written a slew of papers proposing new programming models, file systems, libraries, and applications built to exploit the performance and flexibility that NVDIMMs promised to deliver. Those papers drew conclusions and made design decisions without detailed knowledge of how real NVDIMMs would behave or how industry would integrate them into computer architectures. Now that 3D XPoint NVDIMMs are actually here, we can provide detailed performance numbers, concrete guidance for programmers on these systems, reevaluate prior art for performance, and reoptimize persistent memory software for the real 3D XPoint DIMM.

In this paper, we explore the performance properties and characteristics of Intel’s new 3D XPoint DIMM at the micro and macro level. First, we investigate the basic characteristics of the device, taking special note of the particular ways in which its performance is peculiar relative to traditional DRAM or other past methods used to emulate NVM. From these observations, we recommend a set of best practices to maximize the performance of the device. With our improved understanding, we then explore the performance of prior art in application-level software for persistent memory, taking note of where their performance was influenced by our guidelines.

1 Introduction

Over the past ten years, researchers have been anticipating the arrival of commercially available, scalable non-volatile main memory (NVMM) technologies that provide “byte-addressable” storage that survives power outages. With the arrival of Intel’s Optane DC Persistent Memory Module (which we refer to as 3D XPoint DIMMs), we can start to understand real capabilities, limitations, and characteristics of these memories and starting designing and refining systems to fully leverage them.

We have characterized the performance and behavior of 3D XPoint DIMMs using a wide range of micro-benchmarks, benchmarks, and applications. The data we have collected demonstrate that many of the assumptions that researchers have made about how NVDIMMs would behave and perform are incorrect.

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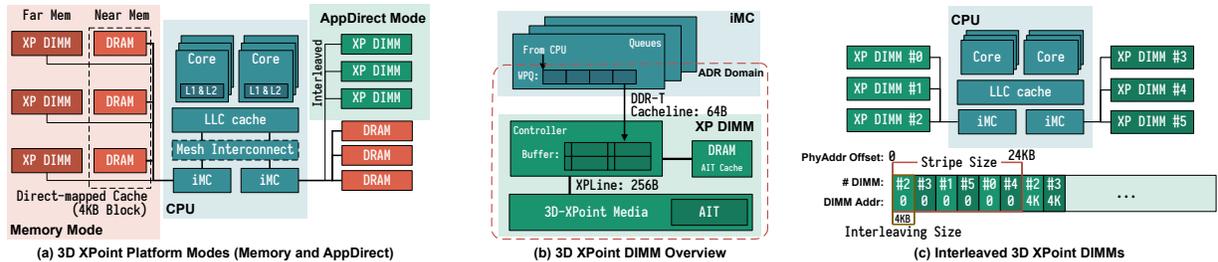


Figure 1: Overview of (a) 3D XPoint platform, (b) 3D XPoint DIMM and (c) how 3D XPoint memories interleave across channels 3D XPoint DIMM can work as volatile far memory with DRAM as cache or persistent memory for application accesses.

The widely expressed expectation was that NVDIMMs would have behavior that was broadly similar to DRAM-based DIMMs but with lower performance (i.e., higher latency and lower bandwidth). These assumptions are reflected in the methodology that research studies used to emulate NVDIMMs, which include specialized hardware platforms [21], software emulation mechanisms [49, 53, 12, 36, 41], exploiting NUMA effects [20, 19, 31], and simply pretending DRAM is persistent [44, 9, 8].

We have found the actual behavior of 3D XPoint DIMMs to be more complicated and nuanced than the “slower, persistent DRAM” label would suggest. 3D XPoint DIMM performance is much more strongly dependent on access size, access type (read vs. write), pattern, and degree of concurrency than DRAM performance. Furthermore, 3D XPoint DIMM’s persistence, combined with the architectural support that Intel’s latest processors provide, leads to a wider range of design choices for software designers.

This paper presents a detailed evaluation of the behavior and performance of 3D XPoint DIMMs on microbenchmarks and applications and provides concrete, actionable guidelines for how programmers should tune their programs to make the best use of these new memories. We describe these guidelines, explore their consequences, and demonstrate their utility by using them to guide the optimization of several NVMM-aware software packages as well as the analysis of previously-published results.

We also compare the behavior of real 3D XPoint DIMMs with several methods researchers have used to emulate persistent main memory (e.g., using custom hardware, exploiting NUMA effects, and pretending DRAM is persistent). We find that all of these emulation methodologies are inaccurate, suggesting that it is unwise to assume that previously published results based on those methodologies reflect performance on real hardware.

The paper proceeds as follows. Section 2 provides architectural details on our test machine and the 3D XPoint DIMM. Section 3 presents experiments on microarchitectural details and parameters, and Section 4 provides a special focus on how the 3D XPoint DIMM is different from DRAM and other emulation techniques. Section 5 uses these results to posit best practices for programmers on the 3D XPoint DIMM. In this section, we first justify each guideline with a micro-benchmark demonstrating the root cause. We then present one or more case studies of how the guideline would (and, in some cases, did) influence a previously proposed 3D XPoint-aware software system. Section 6 provides discussion as to how our guidelines extend to future generations of NVM. Section 7 describes related work in this space, and Section 8 concludes.

2 Background and Methodology

In this section, we provide background on Intel’s 3D XPoint DIMM, describe the test system, and then describe the configurations we use throughout the rest of the paper.

2.1 3D XPoint Memory

The 3D XPoint DIMM is the first scalable, commercially available NVDIMM. Compared to existing storage devices (including the Optane SSDs) that connect to an external interface such as PCIe, the 3D XPoint DIMM has lower latency, higher read bandwidth, and presents a memory address-based interface instead of a block-based NVMe interface. Compared to DRAM, it has higher density and persistence. At its debut, the 3D XPoint DIMM is available in three different capacities: 128, 256, and 512 GB.

2.1.1 Intel’s 3D XPoint DIMM

Like traditional DRAM DIMMs, the 3D XPoint DIMM sits on the memory bus, and connects to the processor’s integrated memory controller (iMC) (Figure 1(a)). Intel’s Cascade Lake processors are the first (and only) CPUs to support 3D XPoint DIMM. On this platform, each processor contains one or two processor dies which comprise separate NUMA nodes. Each processor die has two iMCs, and each iMC supports three channels. Therefore, in total, a processor die can support a total of six 3D XPoint DIMMs across its two iMCs.

To ensure persistence, the iMC sits within the *asynchronous DRAM refresh (ADR)* domain — Intel’s ADR feature ensures that CPU stores that reach the ADR domain will survive a power failure (i.e., will be flushed to the NVDIMM within the hold-up time, $< 100 \mu\text{s}$)[48]. The iMC maintains read and write pending queues (RPQs and WPQs) for each of the 3D XPoint DIMMs (Figure 1(b)), and the ADR domain includes WPQs. Once data reaches the WPQs, the ADR ensures that the iMC will flush the updates to 3D XPoint media on power failure. The ADR domain does not include the processor caches, so stores are only persistent once they reach the WPQs.

The iMC communicates with the 3D XPoint DIMM using the DDR-T interface in cache-line (64-byte) granularity. This interface shares a mechanical and electrical interface with DDR4 but uses a different protocol that allows for asynchronous command and data timing since 3D XPoint memory access latencies are not deterministic.

Memory accesses to the NVDIMM (Figure 1(b)) arrive first at the on-DIMM controller (referred as *XPController* in this paper), which coordinates access to the 3D XPoint media. Similar to SSDs, the 3D XPoint DIMM performs an internal address translation for wear-leveling and bad-block management, and maintains an *address indirection table (AIT)* for this translation [7].

After address translation, the actual access to storage media occurs. As the 3D XPoint physical media access granularity is 256 bytes (referred as *XPLine* in this paper), the XPController will translate smaller requests into larger 256-byte accesses, causing write amplification as small stores become read-modify-write operations. The XPController has a small write-combining buffer (referred as *XPBuffer* in this paper), to merge adjacent writes.

It is important to note that all updates that reach the XPBuffer are already persistent since XPBuffer resides within the ADR. Consequently, the NVDIMM can buffer and merge updates regardless of ordering requirements that the program specifies with memory fences.

2.1.2 Operation Modes

3D XPoint DIMMs can operate in two modes (Figure 1(a)): Memory and App Direct.

Memory mode uses 3D XPoint to expand main memory capacity without persistence. It combines a 3D XPoint DIMM with a conventional DRAM DIMM on the same memory channel that serves as a direct-mapped cache for the NVDIMM. The cache block size is 64 B, and the CPU’s memory controller manages the cache transparently. The CPU and operating system simply see the 3D XPoint DIMM as a larger (volatile) portion of main memory.

App Direct mode provides persistence and does not use a DRAM cache. The 3D XPoint DIMM appears as a separate, persistent memory device. The system can install a file system or other management layer on the device to provide allocation, naming, and access to persistent data. 3D XPoint-aware applications and file systems can access the 3D XPoint DIMMs with load and store instructions.

In App Direct mode, programmers can directly modify the 3D XPoint DIMM’s contents using store instructions, and those stores will, eventually, become persistent. The cache hierarchy, however, can reorder stores, making recovery after a crash challenging [46, 28, 12, 37, 55].

Intel processors offer programmers a number of options to control store ordering. The instruction set provides `clflush` and `clflushopt` instructions to flush cache lines back to memory, and `clwb` can write back (but not

evict) cache lines. Alternately, software can use non-temporal stores (`ntstore`) to bypass the cache hierarchy and write directly to memory. All these instructions are non-blocking, so the program must issue an `sfence` to ensure that a previous cache flush, cache write back, or non-temporal store is complete and persistent.

In both modes, 3D XPoint memory can be (optionally) interleaved across channels and DIMMs (Figure 1(c)). On our platform, the only supported interleaving size is 4 KB, which ensures that accesses to a single page fall into a single DIMM. With six DIMMs, an access larger than 24 KB will access all the DIMMs.

2.2 System Description

We perform our experiments on a dual-socket evaluation platform provided by Intel Corporation. The CPUs are 24-core Cascade Lake engineering samples with the similar spec as the previous-generation Xeon Platinum 8160. Each CPU has two iMCs and six memory channels (three channels per iMC). A 32 GB Micron DDR4 DIMM and a 256 GB Intel 3D XPoint DIMM attach to each of the memory channels. Thus the system has 384 GB (2 socket \times 6 channel \times 32 GB/DIMM) of DRAM, and 3 TB (2 socket \times 6 channel \times 256 GB/DIMM) of NVMM. Our machine runs Fedora 27 with Linux kernel version 4.13.0 built from source.

2.3 Experimental Configurations

As the 3D XPoint DIMM is both persistent and byte-addressable, it can fill the role of either a main memory device (i.e., replacing DRAM) or a persistent device (i.e., replacing disk). In this paper, we focus on the persistent usage, and discuss how our findings apply to using 3D XPoint DIMM as volatile memory in Section 6.

Linux manages persistent memory by creating `pmem` namespaces over a contiguous span of physical memory. A namespace can be backed by interleaved or non-interleaved 3D XPoint memory, or emulated persistent memory backed by DRAM. In this study, we configure the 3D XPoint memory in App Direct mode and create a namespace for each type of memory.

Our baseline (referred as *Optane*) exposes six 3D XPoint DIMMs from the same socket as a single interleaved namespace. In our experiments, we use local accesses (i.e., from the same NUMA node) as the baseline to compare with one or more other configurations, such as access to 3D XPoint memory on the remote socket (*Optane-Remote*) or DRAM on the local or remote socket (*DRAM* and *DRAM-Remote*). To better understand the raw performance of 3D XPoint memory without interleaving, we also create a namespace consisting of a single 3D XPoint DIMM and denote it as *Optane-NI*.

3 Performance Characterization

In this section, we measure 3D XPoint’s performance along multiple axes to provide the intuition and data that programmers and system designers will need to effectively utilize 3D XPoint. We find that 3D XPoint’s performance characteristics are complex and surprising in many ways, especially relative the notion that persistent memory behaves like slightly-slower DRAM.

3.1 LATTester

Characterizing 3D XPoint memory is challenging for two reasons. First, the underlying technology has major differences from DRAM but publicly-available documentation is scarce. Secondly, existing tools measure memory performance primarily as a function of locality and access size, but we have found that 3D XPoint performance depends strongly on memory interleaving and concurrency as well. Persistence adds an additional layer of complexity for performance measurements.

To fully understand the behavior of the 3D XPoint memory, we built a microbenchmark toolkit called LATTester. To accurately measure the CPU cycle count and minimize the impact from the virtual memory system, LATTester runs as a dummy file system in the kernel and accesses pre-populated (i.e., no page-faults) kernel virtual addresses of 3D XPoint DIMMs. LATTester also pins the kernel threads to fixed CPU cores and disables IRQ and cache prefetcher.

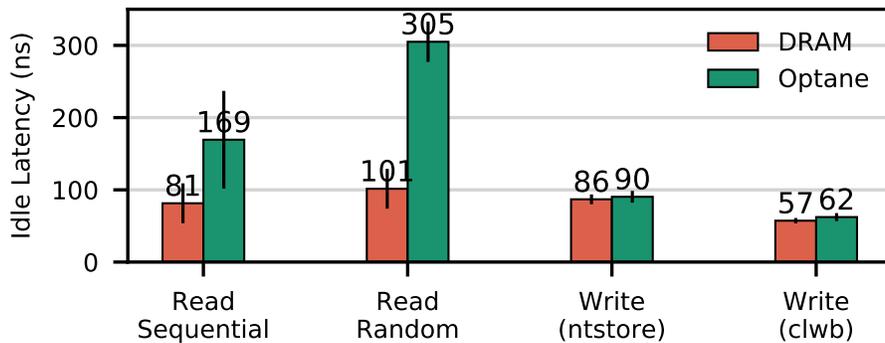


Figure 2: **Best-case latency** An experiment showing random and sequential read latency, as well as write latency using cached write with `clwb` and `ntstore` instructions. Error bars show one standard deviation.

In addition to simple latency and bandwidth measurements, LATTester collects a large set of hardware counters at both the CPU and NVDIMM.

Our investigation of 3D XPoint memory behavior proceeds in two phases. First, we perform a broad, systematic “sweep” over 3D XPoint configuration parameters including access patterns (random vs. sequential), operations (loads, stores, fences, etc.), access size, stride size, power budget, NUMA configuration, and address space interleaving.

Then, we design targeted experiments to investigate anomalies in that data and verify or disprove our hypotheses about the underlying cause. Between our initial sweep and the follow-up tests, we collected over ten thousand data points.

3.2 Typical Latency

Read and write latencies are key memory technology parameters. We measure read latency by timing the average latency for individual 8-byte load instructions to sequential and random memory addresses. To eliminate caching and queuing effects, we empty the CPU pipeline and issue a memory fence (`mfence`) between measurements (`mfence` serves the purpose of serialization for reading timestamps). For writes, we load the cache line into the cache and then measure the latency of one of two instruction sequences: a 64-bit store, a `clwb`, and an `mfence`; or a non-temporal store followed by an `mfence`.

These measurements reflect the load and store latency as seen by software rather than those of these underlying memory device. For loads, the latency includes the delay from the on-chip interconnect, iMC, XPController and the actual 3D XPoint media. Our results (Figure 2) show the read latency for 3D XPoint is $2\times$ – $3\times$ higher than DRAM. We believe most of this difference is due to 3D XPoint having a longer media latency. 3D XPoint memory is also more pattern-dependent than DRAM. The random-vs-sequential gap is 20% for DRAM but 80% for 3D XPoint memory, and we believe this gap is a consequence of the XPBuffer. For stores, the memory store and fence instructions commit once the data reaches the ADR at the iMC. Both DRAM and 3D XPoint memory show a similar latency. Non-temporal stores are more expensive than writes with cache flushes (`clwb`).

In general, the latency variance for 3D XPoint is extremely small, save for an extremely small number of “outliers”, which we investigate in the next section. The sequential read latencies for 3D XPoint DIMMs have higher variances, as the first cache line access loads the entire XPLine into XPBuffer, and the following three accesses read data in the buffer.

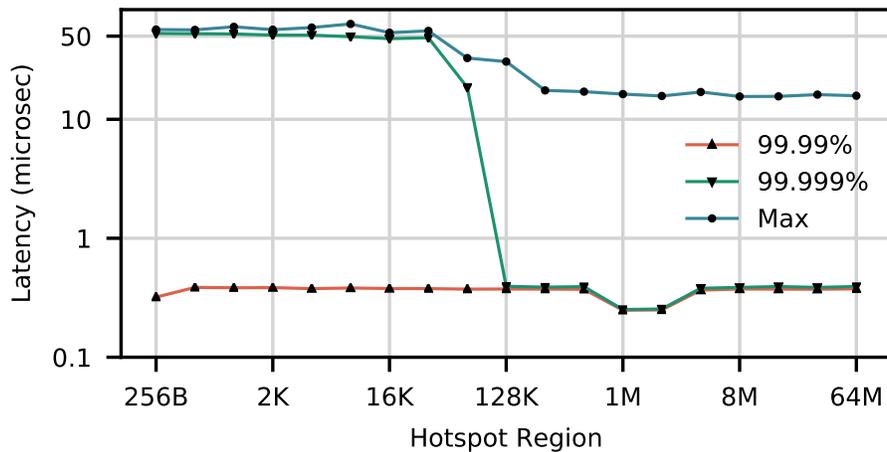


Figure 3: **Tail latency** An experiment showing the tail latency of writing to a small area of memory (hotspot) sequentially. 3D XPoint memory has rare ‘outliers’ where a small number of writes take up to $50 \mu\text{s}$ to complete (an increase of $100\times$ over the usual latency).

3.3 Tail Latency

Memory and storage system tail latency critically affects response times and worst-case behavior in many systems. In our tests, we observed a very consistent latency for loads and stores except a few “outliers”, which increase in number for stores when accesses are concentrated in a “hot spot”.

Figure 3 measures the relationship between tail latency and access locality. The graph shows the 99.9th, 99.99th, and maximal latencies as a function of hot spot size. The number of outliers (especially for the ones over $50\mu\text{s}$) reduces as the hotspot size increases and do not exist for DRAM.

These spikes are rare (0.006% of the accesses), but their latency are 2 orders of magnitude higher than a common case 3D XPoint access. We suspect this effect is due to remapping for wear-leveling or thermal concerns, but we cannot be sure.

3.4 Bandwidth

Detailed bandwidth measurements are useful to application designers as they provide insight into how a memory technology will impact overall system throughput. First, we measure 3D XPoint and DRAM bandwidth for random and sequential reads and writes under different levels of concurrency.

Figure 4 shows the bandwidth achieved at different thread counts for sequential accesses with 256 B access granularity. We show loads and stores (`Write(ntstore)`), as well as cached writes with flushes (`Write(clwb)`). All experiments use AVX-512 instructions and access the data at 64 B granularity. The left-most graph plots performance for interleaved DRAM accesses, while the center and right-most graphs plot performance for non-interleaved and interleaved 3D XPoint. In the non-interleaved measurements all the accesses go to a single DIMM.

Figure 5 shows how performance varies with access size. The graphs plot aggregate bandwidth for random accesses of a given size. We use the best-performing thread count for each curve (given as “load thread count;/ntstore thread count;/store+clwb thread count;” in the figure). Note that the best performing thread count for Optane(Read) varies with different access sizes for random accesses, where 16 threads show good performance consistently.

The data shows that DRAM bandwidth is both significantly higher than 3D XPoint and scales predictably (and monotonically) with thread count until it saturates the DRAM’s bandwidth and that bandwidth is mostly independent of access size.

The results for 3D XPoint are wildly different. First, for a single DIMM, the maximal read bandwidth is $2.9\times$ of

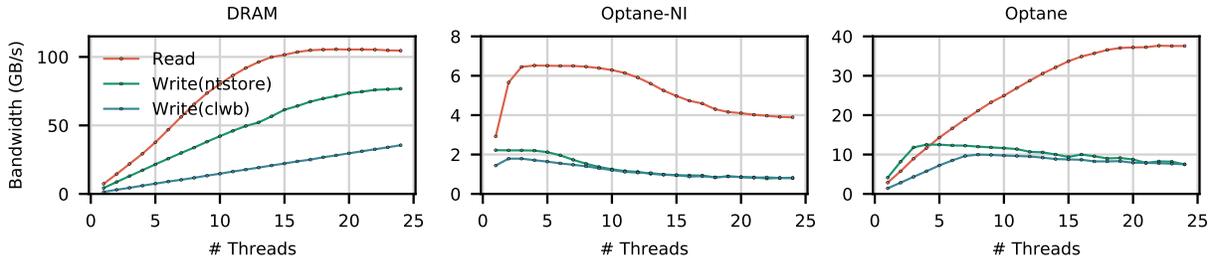


Figure 4: **Bandwidth vs. thread count** An experiment showing maximal bandwidth as thread count increases (from left to right) on local DRAM, non-interleaved and interleaved 3D XPoint memory. All threads use a 256 B access size. (Note the difference in vertical scales).

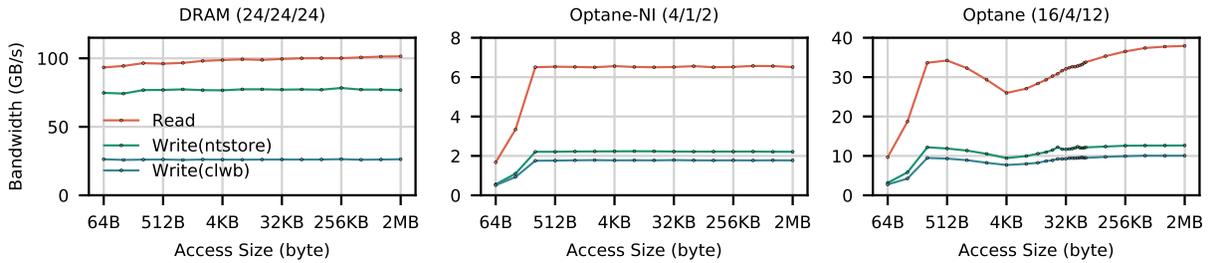


Figure 5: **Bandwidth over access size** An experiment showing maximal bandwidth over different access sizes on (from left to right) local DRAM, interleaved and non-interleaved 3D XPoint memory. Graph titles include the number of threads used in each experiment (Read/Write (ntstore) /Write (clwb)).

the maximal write bandwidth (6.6 GB/s and 2.3 GB/s respectively), where DRAM has a smaller gap (1.3 \times) between read and write bandwidth.

Second, with the exception of interleaved reads, 3D XPoint performance is non-monotonic with increasing thread count. For the non-interleaved (i.e., single-DIMM) cases, performance peaks at between one and four threads and then tails off. Interleaving pushes the peak to twelve threads for `store+clwb`. We will return to the negative impact of rising thread count on performance in Section 5.1.

Third, 3D XPoint bandwidth for random accesses under 256 B is poor. This “knee” corresponds to XPLine size. DRAM bandwidth does not exhibit a similar “knee” at 8 kB (the typical DRAM page size), because the cost of opening a page of DRAM is much lower than accessing a new page of 3D XPoint.

Interleaving (which spreads accesses across all six DIMMs) adds further complexity: Figure 4(right) and Figure 5(right) measure bandwidth across six interleaved NVDIMMs. Interleaving improves peak read and write bandwidth by 5.8 \times and 5.6 \times , respectively. These speedups match the number of DIMMs in the system and highlight the per-DIMM bandwidth limitations of 3D XPoint. The most striking feature of the graph is a dip in performance at 4 KB — this dip is an emergent effect caused by contention at the iMC, and it is maximized when threads perform random accesses close to the interleaving size. We will further discuss the cause and solution of this issue in Section 5.3.

3.5 Latency Under Load

In most systems, latency increases slowly as bandwidth rises until it reaches a “wall” and queuing effects cause latency to rise sharply. To explore this effect in 3D XPoint and DRAM, we use LATTester to vary the offered load to each type of memory. We use the thread counts that get consistently good performance across access sizes. For loads, we use 16 threads. For non-temporal stores, we use 4 threads. Each thread performs cache line sized memory accesses and delays for a set interval between two accesses. Figure 6 plots the results as we vary the delay interval from 0 to 80 μ s.

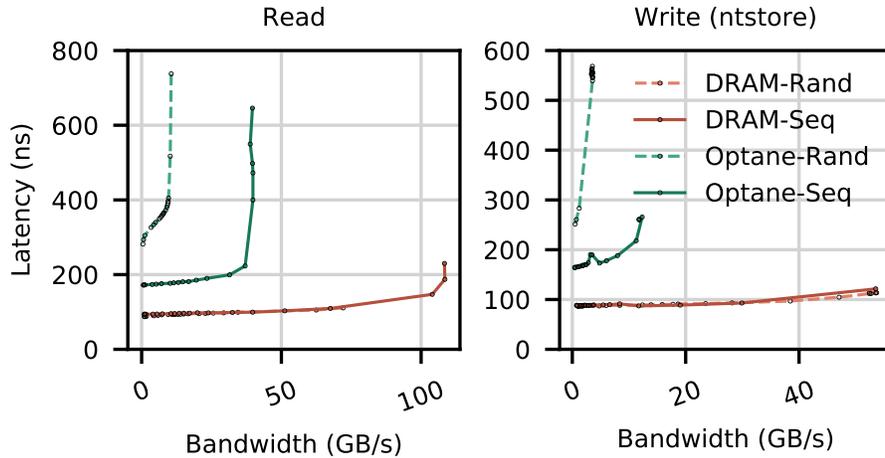


Figure 6: **Memory latency and bandwidth under varying load** The “knee” in the graph occurs when the device begins to suffer from queuing effects and maximum bandwidth is reached. DRAM memory performance is consistent between sequential and random accesses, while 3D XPoint memory is much more sensitive to the access pattern.

The data shows that both DRAM and 3D XPoint behave as expected. The “wall” occurs earlier for 3D XPoint and the latencies are significantly higher. 3D XPoint also shows an imbalance between sequential and random access patterns, unlike DRAM.

4 Comparison to Emulation

Non-volatile memory research has been popular in recent years (e.g. [44, 55, 9, 60, 62, 46, 33, 36, 66, 41, 18, 57, 49, 28]). However, since scalable NVDIMMs have not been available, most of the NVM based systems have been evaluated on emulated NVM. Common ways to emulate NVM include adding delays to memory accesses in software [55, 36, 41], using software emulators [49, 53], using software simulation [46, 33, 12], using hardware emulators such as Intel’s Persistent Memory Emulator Platform (PMEP) [21] to limit latency and bandwidth [66, 61, 60], using DRAM on a remote socket (DRAM-Remote) [19, 31, 20], underclocking DRAM [28] or just using plain DRAM [44, 9, 62, 38] or battery-backed DRAM [18].

Below, we compare these emulation techniques to real 3D XPoint using microbenchmarks and then provide a case study in how those differences can affect research results.

4.1 Microbenchmarks in Emulation

Figure 7(left) shows the write latency/bandwidth curves for NVM emulation mechanisms (e.g. PMEP, DRAM-Remote, DRAM) in comparison to real 3D XPoint memory (similar to Figure 6). Figure 7(right) shows bandwidth with respect to the number of reader/writer threads (all experiments use a fixed number of threads that give maximum bandwidth). Our PMEP configuration adds a 300 ns latency on load instructions and throttles write bandwidth at 1/8 of DRAM bandwidth as this configuration is the standard used in previous works [60, 61, 66, 65]. Note that PMEP is a specialized hardware platform, so its performance numbers are not directly comparable to the system we use in our other experiments.

The data in these figures shows that none of the emulation mechanism captures the details of 3D XPoint’s behavior — all methods deviate drastically in their performance from real 3D XPoint memory. They fail to capture 3D XPoint memory’s preference for sequential accesses and read/write asymmetry and give wildly inaccurate guesses for device latency and bandwidth.

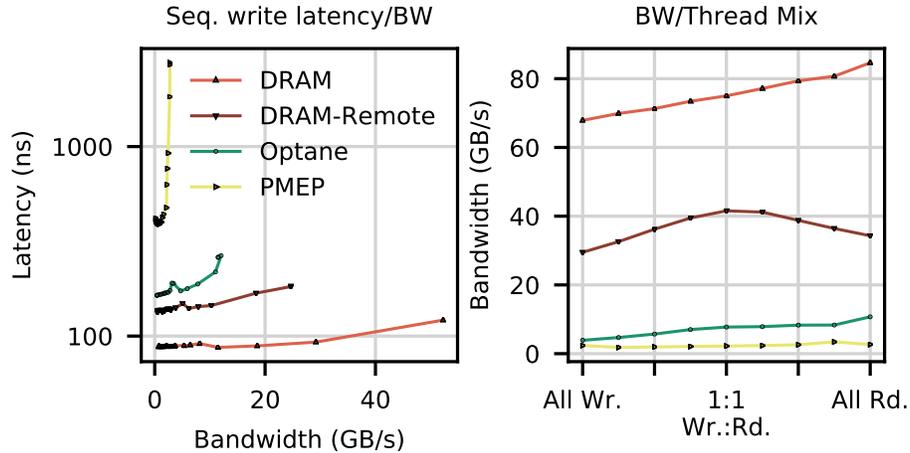


Figure 7: **Microbenchmarks under emulation** The emulation mechanisms used to evaluate many projects do not accurately capture the complexities of 3D XPoint performance.

4.2 Case Study: Optimizing RocksDB

The lack of emulation fidelity can have a dramatic effect on the performance of software. Results may be misleading, especially those based on simple DRAM. In this section, we revisit prior art in NVM programming in order to demonstrate that emulation is generally insufficient to capture the performance of 3D XPoint DIMMs and that future work should be validated on real hardware.

RocksDB [22] is a high-performance embedded key-value store, designed by Facebook and inspired by Google’s LevelDB [16]. RocksDB’s design is centered around the log-structured merge tree (LSM-tree), which is designed for block-based storage devices, absorbing random writes and converting them to sequential writes to maximize hard disk bandwidth.

A recent study [59] compared two strategies for adapting RocksDB to use persistent memory. The first uses a fine-grained persistence approach to migrate RocksDB’s “memtable” to persistent memory, eliminating the need for a file-based write-ahead log. The second approach moved the write-ahead log to persistent memory and used a simpler acceleration technique called FLEX to move logging performance.

The study used DRAM as a stand-in for 3D XPoint, and found that fine-grained persistence offered 19% better performance.

We replicated these experiments on real 3D XPoint media. We used the RocksDB test `db_bench` on SET throughput with 20-byte key size and 100-byte value size, and sync the database after each SET operation; the results are shown in Figure 8. With real 3D XPoint, the result is the opposite: FLEX performs better than fine-grained persistence by 10%. These results are not surprising given 3D XPoint memory’s preference for sequential accesses and its problem with small random writes.

4.3 Discussion

We make two broader observations about our results. First, the differences between emulated and real persistent memory are large enough to alter the conclusions that researchers might draw from their experiments. Second, there does not appear to be any simple relationship between emulated results and results on real 3D XPoint hardware.

We conclude that basing future designs (and design decisions) on the results of emulation-based studies may cause system designers to overlook superior options. It also demonstrates the value of re-evaluating previously considered (and perhaps discarded) ideas on new hardware.

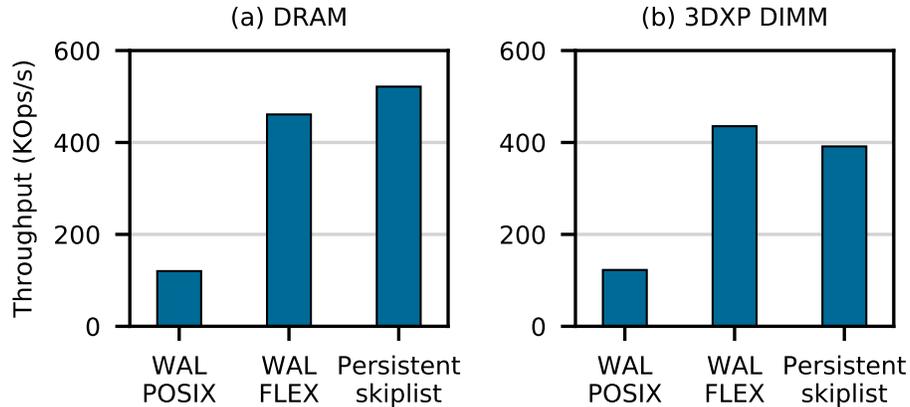


Figure 8: **Migrating RocksDB to 3D XPoint Memory** 3D XPoint media is sufficiently different from DRAM to invert prior conclusions. Using a persistent memtable works best for DRAM emulating persistent memory, but on real 3D XPoint memory the conclusion is reversed.

5 Best Practices for 3D XPoint DIMMs

Section 3 highlights the many differences between 3D XPoint and conventional storage and memory technologies, and Section 4 shows how these differences can manifest to invalidate macro-level results. These differences mean that existing intuitions about how to optimize software for disks and memory do not apply directly to 3D XPoint. This section distills the results of our characterization experiments into a set of four principles for how to build and tune 3D XPoint-based systems.

1. **Avoid random accesses smaller than < 256 B.**
2. **Use non-temporal stores when possible for large transfers, and control of cache evictions.**
3. **Limit the number of concurrent threads accessing a 3D XPoint DIMM.**
4. **Avoid NUMA accesses (especially read-modify-write sequences).**

Below, we describe the guidelines in detail, give examples of how to implement them, and provide case studies in their application.

5.1 Avoid small random accesses

Internally, 3D XPoint DIMMs update 3D XPoint contents at a 256 B granularity. This granularity, combined with a large internal store latency, means that smaller updates are inefficient since they require the DIMM to perform an internal read-modify-write operation causing write amplification. The less locality the accesses exhibit, the more severe the performance impact.

To characterize the impact of small stores, we perform two experiments. First, we quantify the inefficiency of small stores using a metric we have found useful in our study of 3D XPoint. The *Effective Write Ratio (EWR)* is the ratio of bytes issued by the iMC divided by the number of bytes actually written to the 3D XPoint media (as measured by the DIMM’s hardware counters). EWR is the inverse of write amplification.

EWR values below one indicate the 3D XPoint DIMM is operating inefficiently since it is writing more data internally than the application requested. The EWR can be greater than one, due to write-combining at the XPBuffer or DRAM caching (when the 3D XPoint is operating in Memory Mode).

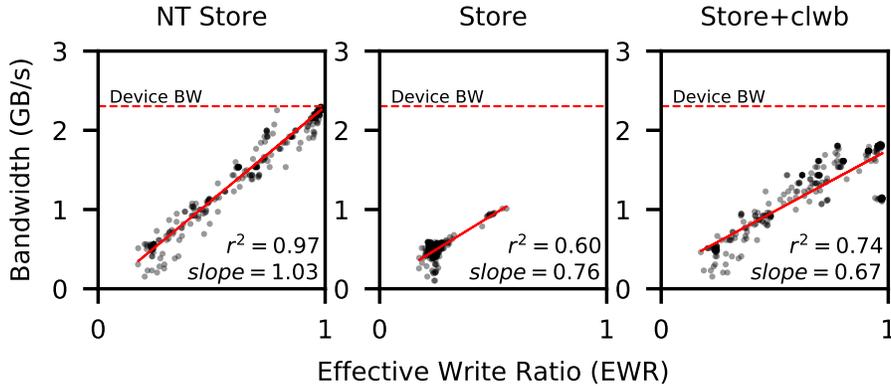


Figure 9: **Relationship between EWR and throughput on a single DIMM** Each dot represents an experiment with different access size, thread count and power budget configurations. Note the correlation between the metrics.

Figure 9 plots the strong correlation between EWR and effective device bandwidth for a single DIMM for all the measurements in our systematic sweep of 3D XPoint performance. Based on this relationship, we conclude that working to maximize EWR is a good way to maximize bandwidth.

In general, small stores exhibit EWR’s of less than one. For example, when using a single thread to perform non-temporal stores to random accesses, it achieves an EWR of 0.25 for 64-byte accesses and 0.98 for 256-byte accesses.

Notably, 256-byte updates are efficient, even though the iMC only issues 64 B to accesses the DIMM — the XPBuffer is responsible for buffering and combining 64 B accesses into 256 B internal writes. As a consequence, 3D XPoint DIMMs can efficiently handle small stores, if they exhibit sufficient locality. To understand how much locality is sufficient, we crafted an experiment to measure the size of the XPBuffer. First, we allocate a contiguous region of N XPLines. During each “round” of the experiment, we first update the first half (i.e., 128 B) of each XPLine in turn. Then, we update the second half of each XPLine. We measure the EWR for each round. Figure 10 shows the results.

Below $N = 64$ (that is, a region size of 16 KB), the EWR is near unity, suggesting that the accesses to the second halves are hitting in the XPBuffer. Above $N = 64$, write amplification jumps, indicating a sharp rise in the miss rate. This result implies the XPBuffer is approximately 16 KB in size. Further experiments demonstrate that reads also compete for space in the XPBuffer.

Together these results provide specific guidance for maximizing 3D XPoint store efficiency: Avoid small stores, but if that is not possible, limit the working set to 16 KB per 3D XPoint DIMM.

5.1.1 Case Study: RocksDB

The correlation between EWR bandwidth explains the results for RocksDB seen in Section 4 and Figure 8. The persistent memtable resulted in many small stores with the poor locality, leading to a low EWR of 0.434. In contrast, the FLEX-based optimization of WAL uses sequential (and larger) stores, resulting in an EWR of 0.999.

5.1.2 Case Study: The NOVA filesystem

NOVA [60, 61] is a log-structured, NVMM file system that maintains a separate log for each file and directory and uses copy-on-write for file data updates to ensure data consistency. The original NOVA studies used emulated NVMM for their evaluations, so NOVA has not been tuned for 3D XPoint.

The original NOVA design has two characteristics that degrade performance on 3D XPoint. First, the log entries NOVA appends for each metadata update are small – 40-64 B, and since NOVA uses many logs, log updates exhibit little locality, especially when the file system is under load. Second, NOVA uses copy-on-write to 4 KB pages for file

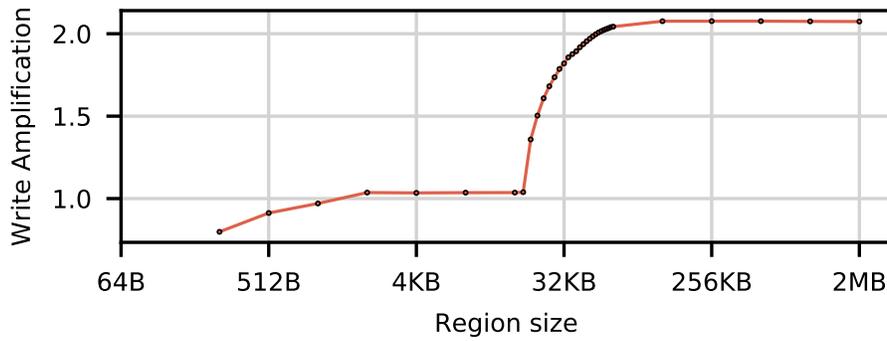


Figure 10: **Inferring XPBuffer capacity** The data show that the 3D XPoint DIMM can use the XPBuffer to coalesce writes spread across up to 64 XPLines.

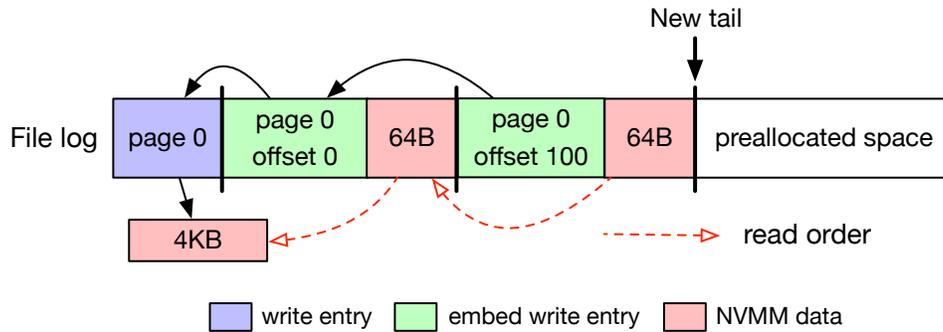


Figure 11: **NOVA-datalog mechanism** Sequentially embedding data along with metadata turns random writes into sequential writes so that it improves small random write speed without giving up atomic file updates. This figure illustrates how NOVA-datalog appends two 64 B random writes (at 0 and 100, respectively) into the log of a 4 KB file.

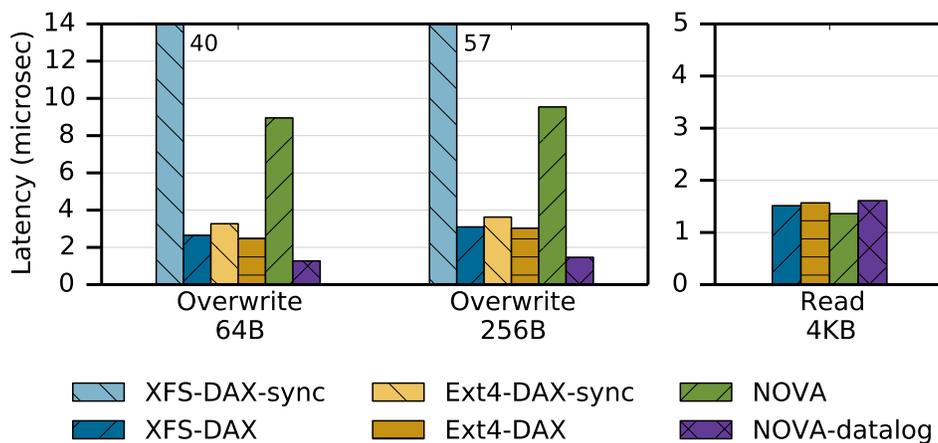


Figure 12: **File IO latency** NOVA-datalog significantly speeds up small random writes, but adds a slight overhead in the read path. Like NOVA and unlike Ext4 or XFS, NOVA-datalog still provides data consistency.

data updates, resulting in useless stores. This inefficiency occurs regardless of the underlying memory technology, but 3D XPoint’s poor store performance exacerbates its effect.

We address both problems by increasing the size of log entries and avoiding some copy-on-write operations. Our modified version of NOVA – *NOVA-datalog* – embeds write data for sub-page writes into the log (Figure 11). Unlike the log’s normal *write entry*, which contains a pointer to a new copy-on-write 4 KB page and its offset within the file, an *embed write entry* contains a page offset, an address within the page, and is followed by the actual contents of the write.

This optimization requires several subsidiary changes to the original NOVA design. In particular, NOVA must merge sub-page updates into the target page before memory-mapping or reading the file. Small changes are also required to the log cleaner to track the liveness of embedded file data.

Figure 12 shows the latencies of random overwrites and reads for three file systems with different modes. For XFS-DAX and Ext4-DAX (the two NVM-based file systems included in Linux), we measure both normal *write* and *write* followed by *fsync* (labeled with “-sync”).

NOVA-datalog improves write performance significantly compared to the original design (by 7×, 6.5× for 64 byte, 256 byte writes, respectively) and meets (for 256 B) or exceeds (for 64 B) performance for the other file systems (which do not provide data consistency). Read latency increases slightly compared to the original NOVA.

EWR measurements generally mirror the performance gains. NOVA-datalog provides the largest gains relative to NOVA because by merging the data into the log it eliminates the discontinuity between writes into the log entry and writes into the file data.

5.2 Use non-temporal stores for large writes

The choice of how programs perform and order updates to 3D XPoint has a large impact on performance. When writing to persistent memory, programmers have several options. After a regular *store*, programmers can either evict (*clflush*, *clflushopt*) or write back (*clwb*) the cache line to move the data into the ADR and eventually into the 3D XPoint DIMM. Alternatively, the *ntstore* instruction can write directly to persistent memory, bypassing the cache hierarchy. For all these instructions, a subsequent *sfence* ensures that the effects of prior evictions, write backs, and non-temporal stores are persistent.

In Figure 13, we compare achieved bandwidth (left) and latency (right) for sequential accesses using AVX-512 store instructions with three different instruction sequences: *ntstore*, *store* + *clwb*, and *store*, followed by a *sfence*. Our bandwidth test uses six threads as it gives good results for all instructions.

The data show that flushing after each 64 B store improves the bandwidth for accesses larger than 64 B. We believe this is because letting the cache naturally evict cache lines adds nondeterminism to the access stream that reaches the 3D XPoint DIMM. Proactively cleaning the cache ensures that accesses remain sequential. The EWR correlates this hypothesis: Adding flush instructions increases the EWR from 0.26 to 0.98.

The data also show that non-temporal stores have lower latency than *store* + *clwb* for accesses over 512 B. Non-temporal stores also have highest bandwidth for accesses over 256 B. Here, we suspect the performance boost is due to the fact that a *store* + *clwb* must load the cache line into the CPU’s local cache before executing *store*, thereby using up some of the 3D XPoint DIMMs bandwidth. As *ntstores* bypass the cache, they will avoid this extraneous read and can achieve higher bandwidth.

In Figure 14, we show how *sfences* affect performance. We use a single thread to issue sequential writes of different sizes on Optane-NI. We issue *clwb* during the write of each cache line (every 64B), or after the entire write (write size). At the end of the write we issue a single *sfence* to ensure the entire write is persistent (we call this entire operation an “*sfence interval*”). The result shows the bandwidth peaks when the write size is 256 B. This peak is a consequence of the semantics of *clflushopt* which is tuned for moderately sized writes [1]. Flushing during or after a medium sized write (beyond 1 KB) does not affect the bandwidth, but when the write size is over 8 MB, flushing after the write causes performance degradation as we incur cache capacity invalidations and a higher EWR.

5.2.1 Case Study: Micro-buffering for PMDK

Our analysis of the relative merits of non-temporal versus normal stores provides us an opportunity to optimize existing work. For example, recent work proposed the “micro-buffering” [64] technique for transactionally updating persistent

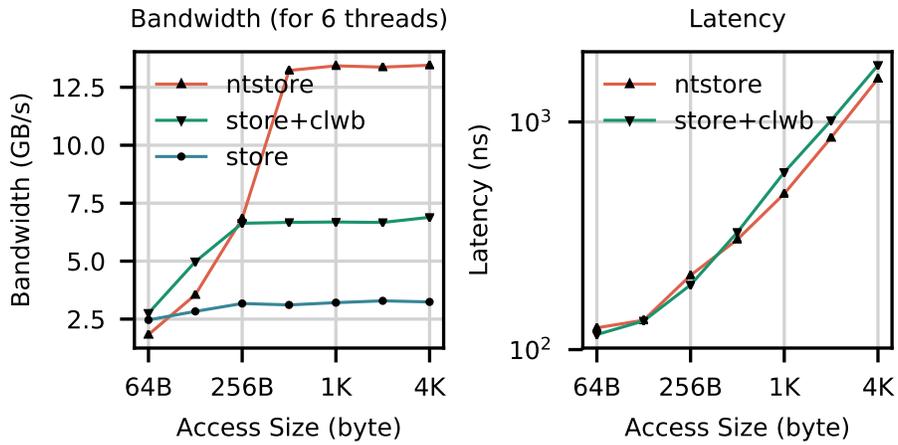


Figure 13: **Performance achievable with persistence instructions** Flush instructions have lower latency for small accesses, but `ntstore` has better latency for larger accesses. Using `ntstore` also avoids an additional read of the cache line from 3D XPoint memory, resulting in higher bandwidth.

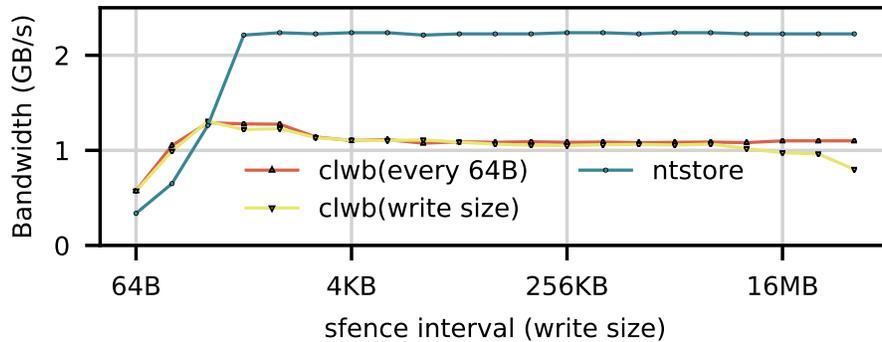


Figure 14: **Bandwidth over sfence intervals.** The bandwidth of 3D XPoint memory decreases when sfence interval increases and when the window of `clwb` causing implicit cache evictions.

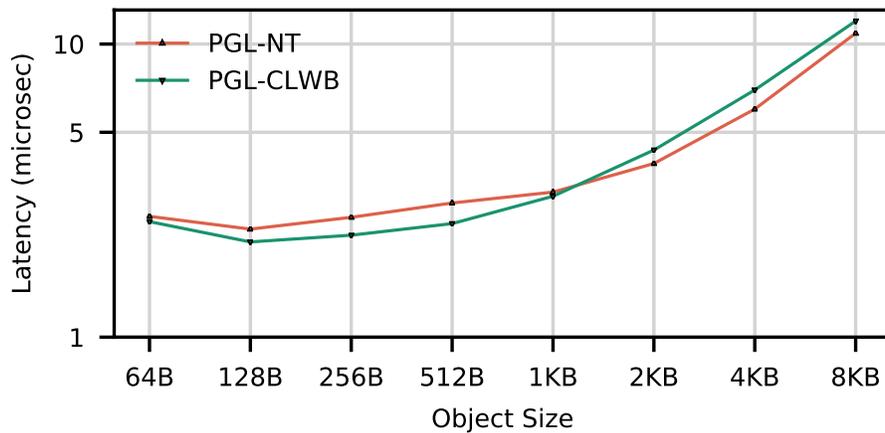


Figure 15: **Tuning persistence instructions for micro-buffering** Using `ntstores` only for large writes, and using `clwb` for small stores can improve performance even at the macro-level.

objects. That work modified the Intel’s PMDK [14] transactional persistent object library to copy objects from 3D XPoint to DRAM at the start of a transaction rather than issuing loads directly to 3D XPoint. On transaction commit, it writes back the entire object at once using non-temporal stores.

The original paper only used non-temporal stores, but our analysis suggests micro-buffering would perform better if it used normal stores for small objects as long as it flushed the affected cache lines immediately after updating them. Figure 15 compares the latency of a no-op transaction for objects of various sizes for unmodified PMDK and micro-buffering with non-temporal and normal store-based write back. The crossover between normal stores and non-temporal stores for micro-buffering occurs at 1 KB.

5.3 Limit the number of concurrent threads accessing a 3D XPoint DIMM

Systems should minimize the number of concurrent threads targeting a single DIMM simultaneously. An 3D XPoint DIMM’s limited store performance and limited buffering at the iMC and on the DIMMs combine to limit its ability to handle accesses from multiple threads simultaneously. We have identified two distinct mechanisms that contribute to this effect.

Contention in the XPBuffer Contention for space in the XPBuffer will lead to increased evictions and write backs to 3D XPoint media, which will drive down EWR. Figure 4(center) shows this effect in action: For example, when using a single thread to issue sequential non-temporal stores, we can achieve an EWR of 0.98. In contrast, when using 8 threads to issue sequential non-temporal stores to private regions of the DIMM, the EWR drops to 0.62.

Contention in the iMC Figure 16 illustrates how limited queue capacity in the iMC also hurts performance when multiple cores target a single DIMM. The figure shows an experiment that uses a fixed number of threads (24 for read and 6 for `ntstore`) to read/write data to 6 interleaved 3D XPoint DIMMs. We let each thread access N DIMM (with even distribution across threads) randomly. As N rises, the number of writers targeting each DIMM grows, but the per-DIMM bandwidth drops. A possible culprit is the limited capacity of the XPBuffer, but EWR remains very close to 1, so the performance problem must be in the iMC.

On our platform, the WPQ buffer in the iMC cannot queue data more than 256 B from a single thread. Our hypothesis is that, since 3D XPoint DIMMs are slow, they drain the WPQ slowly, which leads to head-of-line blocking effects. Increasing N increases contention for the DIMMs and the likelihood that any given processor will block waiting for stores ahead of it to complete.

Figure 5(right) shows another example of this phenomenon — 3D XPoint bandwidth falls drastically when doing

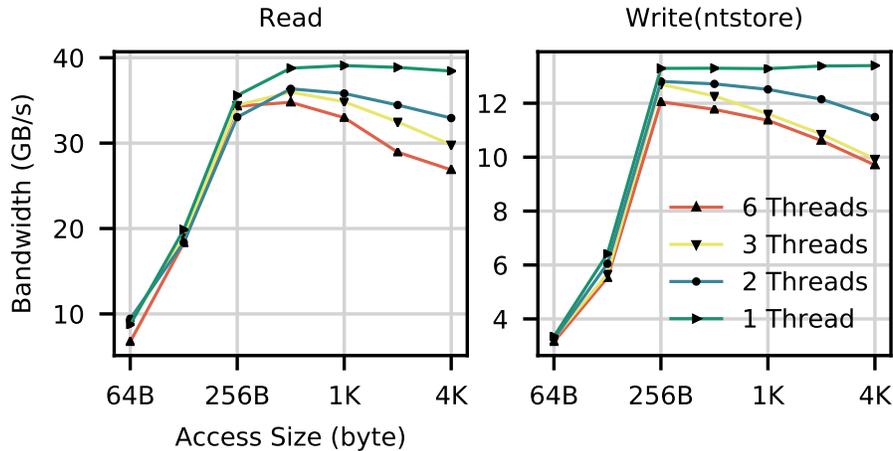


Figure 16: **Plotting iMC contention.** With a fixed number of threads (6), as the number of DIMMs accessed by each thread grows, bandwidth drops. For maximal bandwidth, threads should be pinned to DIMMs.

random 4 KB accesses across interleaved 3D XPoint DIMMs. 3D XPoint memory interleaving is similar to RAID-0 in disk arrays: The chunk size is 4 KB and the stripe size is 24 KB (Across the 6 DIMMs on the socket, each gets a 4 KB contiguous block). The workload in Figure 5(right) spreads accesses across these interleaved DIMMs, and will lead to spikes in contention for particular DIMMs.

Thread starvation occurs more often as the access size grows, reaching maximum degradation at the interleaving size (4 KB). For accesses larger than the interleaving size, each core starts spreading their accesses across multiple DIMMs, evening out the load. The write data also show small peaks at 24 KB and 48 KB where accesses are perfectly distributed across the six DIMMs.

This degradation effect will occur whenever 4 KB accesses are distributed non-uniformly across the DIMMs. Unfortunately, this is probably a common case in practice. For instance, a page buffer with 4 KB pages would probably perform poorly in this configuration.

5.3.1 Case Study: Multi-NVDIMM NOVA

The original NOVA design did not attempt to limit the number of writers per DIMM. In fact, as, it tends to allocate pages for a file from contiguous regions which, via interleaving, tends to spread those pages across the DIMMs. To fix this issue, we configured our machine to pin writer threads to non-interleaved 3D XPoint DIMMs. This configuration ensures an even matching between threads and NVDIMMs, thereby leveling the load and maximizing bandwidth at each NVDIMM.

Figure 17 shows the result. Our experiment uses the FIO benchmark [6] to test the optimization and uses 24 threads. We plot the bandwidth of each file operation with two different IO engines: `sync` and `libaio` (async). By being Multi-NVDIMM aware, our optimization improves NOVA's bandwidth by between 3 and 34%.

5.4 Avoid mixed or multi-threaded accesses to remote NUMA nodes

NUMA effects for 3D XPoint are much larger than they are for DRAM, so designers should work even harder to avoid cross-socket memory traffic. The cost is especially steep for accesses that mix load and stores and include multiple threads. Between local and remote 3D XPoint memory, the typical read latency difference is $1.79\times$ (sequential) and $1.20\times$ (random), respectively. For writes, remote 3D XPoint memory's latency is $2.53\times$ (ntstore) and $1.68\times$ higher compared to local. For bandwidth, remote 3D XPoint can achieve 59.2% and 61.7% of local read and write bandwidth at optimal thread count (16 for local read, 10 for remote read and 4 for local and remote write).

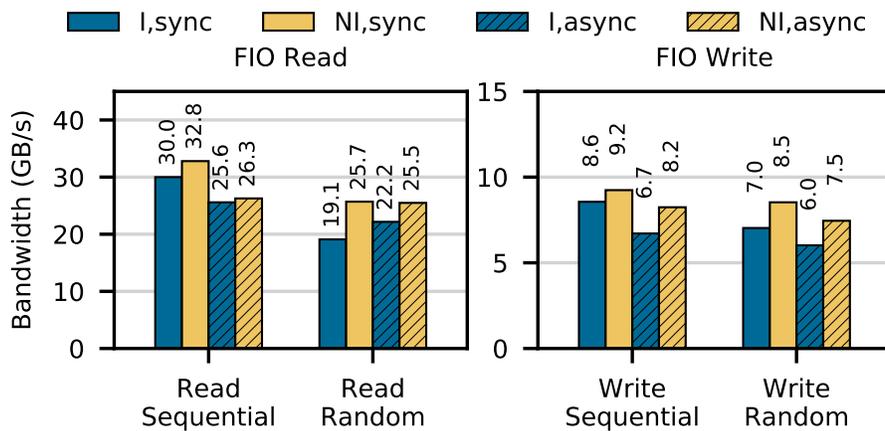


Figure 17: **Multi-DIMM NOVA** Evenly distributing the load across NVDIMMs is important for maximizing application bandwidth. By making NOVA multi-DIMM aware, we improve performance by an average of 17% on the FIO benchmark.

The performance degradation ratio above is similar to remote DRAM to local DRAM. However, the bandwidth of 3D XPoint memory is drastically degraded when either the thread count increases or the workload is read/write mixed. Based on the results from our systematic sweep, the bandwidth gap between local and remote 3D XPoint memory for the same workload can be over 30 \times , while the gap between local and remote DRAM is, at max, only 3.3 \times .

In Figure 18, we show how the bandwidth changes for 3D XPoint on both local and remote CPUs by adjusting the read and write ratio. We show the performance of a single thread and four threads, as local 3D XPoint memory performance increases with thread count up to four threads for all the access patterns tested.

Single-threaded bandwidth is similar for local and remote accesses. For multi-threaded accesses, remote performance drops off much more quickly as store intensity rises, leading much lower performance relative to the local case.

5.4.1 Case Study: PMemKV

Intel’s Persistent Memory Key-Value Store (PMemKV [15]) is an NVMM-optimized key-value data-store. It implements various index data structures (called “storage engines”) to index programs data and uses the Persistent Memory Development Kit (PMDK [14]) to manage its persistent data. We used the concurrent hash map (`cmap`) in our tests as it is the only engine that supports concurrency.

To test the effect of 3D XPoint’s NUMA imbalance on PMemKV, we varied the location of the server relative to the `pmem` pool; Figure 19 shows the result on the included benchmark on a test with mixed workload (`overwrite`) that repeatedly performs read-modify-write operations. In this test, using a remote 3D XPoint DIMM drops the performance of the store beyond two threads. 3D XPoint performance is far more drastically impacted by the migration (loss of 75%) than DRAM (loss of 8%).

6 Discussion

The guidelines in Section 5 provide a starting point for building and tuning 3D XPoint-based systems. By necessity, they reflect the idiosyncrasies of a particular implementation of a particular persistent memory technology, and it is natural to question how applicable the guidelines will be to both other memory technologies and future versions of Intel’s 3D XPoint memory. It is also important to note that we have only studied the guidelines in the context of App Direct mode, since the large DRAM cache that Memory Mode provides mitigates most or all of the effects they

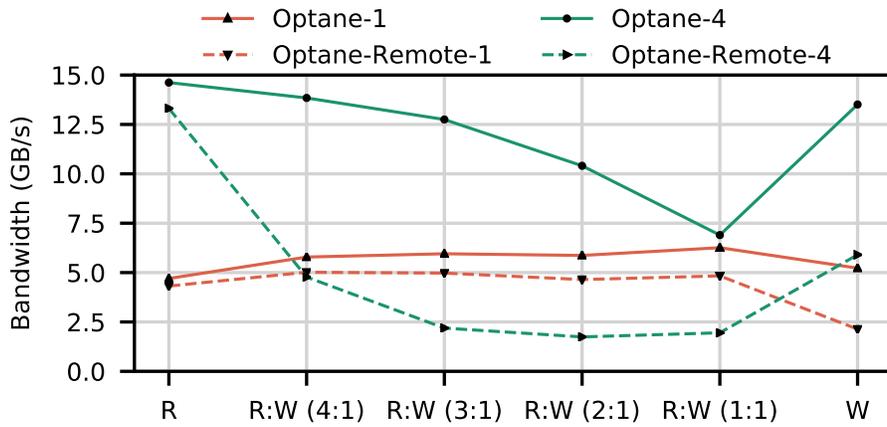


Figure 18: **Memory bandwidth on Optane and Optane-Remote** This chart shows memory bandwidth as we vary the mix of accesses for both one and four threads. Pure reads or pure writes perform better on NUMA than mixed workloads and increased thread count generally hurts NUMA performance.

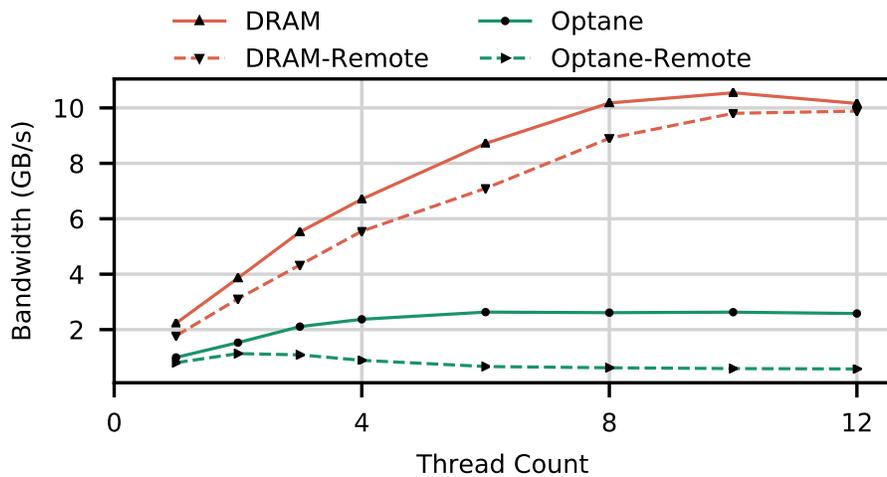


Figure 19: **NUMA degradation for PmemKV** 3D XPoint memory experiences greater NUMA-based degradation than DRAM. In our experiments, migrating to a remote 3D XPoint node reduces the performance of the persistent key-value store PmemKV by up to $4.5\times$ ($18\times$ versus DRAM)

account for. We believe that our guidelines will remain valuable both as 3D XPoint evolves and as other persistent memories come to market.

The broadest contribution of our analysis and the resulting guidelines is that they provide a road map to potential performance problems that might arise in future persistent memories and the systems that use them. Our analysis shows how and why issues like interleaving, buffering on and off the DIMM, and instruction choice, concurrency, and cross-core interference can affect performance. If future technologies are not subject to the precisely the same performance pathologies as 3D XPoint, they may be subject to similar ones.

Ultimately it is unclear how commercially available, scalable persistent memories will evolve. Several of our guidelines are the direct product of (micro)architectural characteristics of the current 3D XPoint incarnation. The size of the XPBuffer and iMC's WPQ might change in future implementations, which would limit the importance of minimizing concurrent threads and reduce the importance of the 256 B write granularity. However, expanding these structures would increase the energy reserves required to drain the ADR during a power failure. Despite this, there are proposals to extend the ADR down to the last-level cache [43, 67] which would eliminate the problem. An even more energy-intensive change would be to make the DRAM cache that 3D XPoint uses in Memory mode persistent.

Increasing or decreasing the 256 B internal write size is likely to be expensive. It is widely believed that 3D XPoint is phase-change memory and the small internal page size has long been a hallmark of the phase change memory [2] due to power limitations. Smaller internal page sizes are unlikely because the resulting memories are less dense.

A different underlying memory cell technology (e.g., spin-torque MRAM) would change things more drastically. Indeed, battery-backed DRAM is a well-known and widely deployed (although not very scalable or cost-effective) persistent memory technology. For it, most of our guidelines are no longer needed, although non-temporal stores are still more efficient for large transfers due to the restrictions of the cache coherency model.

7 Related Work

With the release of the 3D XPoint DIMM in April 2019, early results on the devices have begun to be published. For instance, Van Renan et al. [50] have explored logging mechanisms for the devices, and Izraelevitz et al. [30] have explored general performance characteristics. We expect additional results to be published in the near future as the devices become more widely available.

Prior art in persistent memory programming has spanned the system stack, though until very recently these results were untested on real 3D XPoint media. A large body of work has explored transactional memory-type abstractions for enforcing a consistent persistent state [55, 12, 9, 28, 5, 37, 26, 25, 40]. Various authors have built intricate NVM data structures for data storage and transaction processing [45, 63, 11, 10, 44, 29, 24, 3, 39, 51]. Recent research on in-memory databases has also investigated NVM-based durability. For online transactional processing (OLTP) engines not explicitly designed for NVM, NVM-aware logging [27, 56, 23, 47] and query processing [52] can improve performance. Other authors have investigated speculative techniques for adapting database designs for architectures with NVM [17, 4], while Kimura's FOEDUS [32] builds a custom DBMS for NVM from the ground up. Custom NVM file systems have also been explored [60, 62, 38, 58, 54, 13, 21, 61, 68], as have more speculative hardware architectures [35, 34, 33, 42].

8 Conclusion

This paper has described the performance of Intel's new 3D XPoint DIMMs across micro- and macro-level benchmarks. In doing so, we have extracted actionable guidelines for programmers to fully utilize these devices strengths. As expected, the devices have performance characteristics that lie in-between traditional storage and memory devices, yet they also present a number of interesting performance pathologies and pitfalls that the programmer must be careful to avoid. That said, we believe that the devices will be useful in extending the quantity of memory available to memory-intensive applications and in providing low-latency storage to high performance applications. Future work remains in migrating existing systems to these devices and designing custom software for their peculiarities.

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